

What is claimed is:

1 1. A semiconductor device, comprising:
2 a semiconductor device body exposing at least one
3 silicon-containing portion;
4 a metal silicide layer with a first resistivity
5 overlying the silicon-containing portion; and
6 a conductor layer with a second resistivity
7 overlying the metal silicide layer, wherein the
8 second resistivity is small than the first
9 resistivity.

1 2. The semiconductor device as claimed in claim 1,
2 wherein the conductor layer comprises the same type metal
3 ion as that of the metal silicide layer.

1 3. The semiconductor device as claimed in claim 1,
2 wherein the conductor layer comprises refractory metal.

1 4. The semiconductor device as claimed in claim 1,
2 wherein the metal silicide layer comprises a silicide of
3 refractory metal.

1 5. The semiconductor device as claimed in claim 1,
2 wherein the conductor layer comprises a metal selected
3 from a group consisting of Au, Pt, Ni, Co, Pd, W and Ti.

1 6. A resistance-reduced transistor, comprising:
2 a silicon substrate having a gate stack formed
3 thereon, wherein the gate stack exposes a
4 silicon gate electrode;
5 a pair of source/drain regions, oppositely disposed
6 in the silicon substrate adjacent the gate
7 stack; and
8 a metallized bilayer overlying each source/drain
9 region and the silicon gate electrode to
10 thereby respectively reduce resistance thereof,
11 wherein the metallized bilayer comprises a
12 metal top layer.

1 7. The transistor as claimed in claim 6, further
2 comprising a metal silicide layer disposed between the
3 metal top layer and each source/drain region and the
4 silicon gate electrode.

1 8. The transistor as claimed in claim 6, wherein
2 the metal top layer comprises the same type of metal ion
3 as that of the metal silicide layer.

1 9. The transistor as claimed in claim 6, wherein
2 the metal top layer comprises refractory metal.

1 10. The transistor as claimed in claim 6, wherein
2 the metal silicide layer comprises a silicide of
3 refractory metal.

1 11. The transistor as claimed in claim 6, wherein
2 the metal top layer comprises metal selected from a group
3 consisting of Au, Pt, Ni, Co, Pd, W and Ti.

1 12. A method of fabricating a semiconductor device,
2 comprising the steps of:

3 providing a semiconductor device body exposing at
4 least one silicon-containing portion;

5 selectively forming a metal silicide layer with a

6 first resistivity over the silicon-containing

7 portion; and

8 forming a conductor layer with a second resistivity
9 on the metal silicide layer, wherein the second
10 resistivity is smaller than the first
11 resistivity.

1 13. The method as claimed in claim 12, wherein the
2 conductor layer comprises the same type of metal ion as
3 that of the metal silicide layer.

1 14. The method as claimed in claim 12, wherein the
2 metal layer comprises refractory metal.

1 15. The method as claimed in claim 12, wherein the
2 conductor silicide layer comprises a silicide of
3 refractory metal.

1 16. The method as claimed in claim 12, wherein the
2 metal layer comprises a metal selected from a group
3 consisting of Au, Pt, Ni, Co, Pd, W and Ti.

1 17. The method as claimed in claim 12, wherein the
2 conductor layer is formed by electroless plating.

1 18. The method as claimed in claim 17, wherein the
2 electroless plating is performed in an electrolyte
3 comprising at least a reducing agent, a catalyst, a
4 complex agent and metal ions of the metal layer.

1 19. The method as claimed in claim 18, wherein the
2 catalyst comprises Pd or metal ions of the conductor
3 layer.

1 20. The method as claimed in claim 12, wherein a
2 thickness ratio between the metal silicide layer and the
3 conductor layer is about 1:1 to 1:10.

1 21. A method of fabricating a resistance-reduced
2 transistor, comprising the steps of:

3 providing a silicon substrate having a gate stack
4 formed thereon and a source/drain pair
5 oppositely formed in each side of the substrate
6 adjacent to the gate stack, wherein the gate
7 stack comprises an exposed silicon gate
8 electrode;

9 selectively forming a metal silicide layer over the
10 source/drain regions and the exposed silicon
11 gate electrode; and

12 selectively forming a metal layer over each metal
13 silicide layer by electroless plating to
14 respectively reduce resistance of each
15 source/drain region and the exposed silicon
16 gate electrode.

1 22. The method as claimed in claim 21, wherein the
2 metal layer comprises the same type of metal ion as that
3 of the metal silicide layer.

1 23. The method as claimed in claim 21, wherein the
2 metal layer comprises refractory metal.

1 24. The method as claimed in claim 21, wherein the
2 metal silicide layer comprises a silicide of refractory
3 metal.

1 25. The method as claimed in claim 21, wherein the
2 metal layer comprises a metal selected from a group
3 consisting of Au, Pt, Ni, Co, Pd, W and Ti.

1 26. The method as claimed in claim 21, wherein the
2 electroless plating is performed in an electrolyte
3 comprising at least a reducing agent, a catalyst, a
4 complex agent and metal ions of the metal layer.

1 27. The method as claimed in claim 26, wherein the
2 catalyst comprises Pd or the metal ions of the metal
3 layer.

1 28. The method as claimed in claim 21, wherein a
2 thickness ratio between the metal silicide layer and the
3 metal layer is about 1:1 to 1:10.